REMARKS

In the above-identified Office Action the Examiner has rejected Claims 1-5 as being unpatentable over the patent to Iida et al. With regard to Claim 1, the Examiner has stated that the ratio G_e/G_c can be determined to be 1.07 with a pulling rate of .72mm./min; however, applicant notes that Iida states that the appropriate pulling rate forming what he terms the end-region was a pulling rate of .55mm./min and thus, if this pulling rate was not maintained, there were regions obtained which had defects. Accordingly, Iida does not teach the values set forth in Claim 1 and thus, Claim 1 and the Claims dependant thereon, i.e. Claims 2-5 should be allowable over Iida.

Examiner has also rejected Claims 1-5 over Hourai et al. Applicant has set forth in the application on pages 12-14 the differences and distinguishes with Hourai. Succinctly put, Hourai appears to teach away from a V/G value of less than .20, as claimed.

Claim 7 has been rejected as being obvious over the patent to Kim et al. in view of the patent to Luter. Applicant has amended Claim 7 so that it now better describes the invention and distinguishes it from Kim et al. and Luter. Kim et al. and Luter do not have the concept of controlling the in-crystal temperature gradient in the pulling axis direction of a silicon single crystal ingot. Neither Kim et al. or Luter have a control means as now recited in Claim 7. As a result, applicant believes Claim 7 to now recite over Kim et al. and Luter. Support for the control means may be found on page 14, line 22 thru page 15, line 8.

Claims 9-13 have been rejected as being unpatentable over the patent to Adachi et al. Applicant has amended Claims 9-11 so that these claims now recite a heat treating method for a relatively defect free silicon single crystal wafer. Adachi et al. is directed to method for annealing wafers having multiple defects, whereas applicant does not treat wafers with defects, rather wafers of relatively defect free characteristics, as now recited in the Claims. Accordingly, applicant does not believe that Adachi et al. is relevant to the subject Claims.

Applicant respectfully submits that the present application, in light of the amendments and the remarks, is in condition for allowance, and such action is earnestly solicited. Should the Examiner determine that there are outstanding issues which may be readily resolved through a telephone interview, the Examiner is invited to contact applicant's undersigned attorney at the telephone number listed below.

Respectfully submitted,

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2/04/03
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Please amend Claims 1-5, 7 and 9-11 as follows:

1. (Amended) A method for producing a relatively defect free silicon single crystal ingot under the following conditions:

   (a) V/G value from a crystal center position to a crystal outer periphery position = 0.16 – 0.18 $mm^2/°C \cdot min$,

   (b) G outer / G center $\leq$ 1.10, where V (mm/min) is a pulling speed in the Czochralski method, G (°C/mm) is an average value of an in-crystal temperature gradient in a pulling axis direction within a temperature range from a silicon melting point to 1350°C, G outer is a G value on an outer surface of the crystal, and G center is a G value at the center of the crystal.

2. (Amended) The method for producing a relatively defect free silicon single crystal ingot according to Claim 1, characterized in that said conditions (a) and (b) are adjusted by changing a distance between a heat shielding element equipped in a Czochralski method-based silicon single crystal production device and silicon melt.

3. (Twice Amended) The method for producing a relatively defect free silicon single crystal ingot according to Claim 1, characterized in that said conditions (a) and (b) are adjusted by changing the pulling speed of the silicon single crystal ingot when the silicon single crystal ingot is produced by the Czochralski method.

4. (Twice Amended) A relatively defect free silicon single crystal wafer with decreased grown-in defects, which is obtained from said silicon single crystal ingot according to Claim 1.

5. (Twice Amended) A relatively defect free silicon perfect single crystal wafer free from grown-in defects, which is obtained from said silicon single crystal ingot according to Claim 1.

7. (Twice Amended) A Czochralski method-based silicon single crystal production device, comprising, in a closed container, a crucible element which stores silicon melt, rotates and is vertically driven, a pulling element for pulling a silicon single crystal ingot, while rotating from said silicon melt, a heating element for heating said crucible, and a heat shielding element for shielding radiating heat from said heating element, [characterized in that a drive mechanism for moving said heat shielding element is equipped for changing an in-crystal temperature gradient in a pulling axis direction of the silicon single crystal ingot and for adjusting a ration V/G of a pulling speed V in the Czochralski method to an average value G of the in-crystal temperature gradient in a pulling axis direction within a temperature

range from the silicon melting point to 1350°C to be within a range of 0.16 to $0.18mm^2/°Cmm$. and a ratio of G outer/G center is 1.10 or less, where G outer and G center are the temperature at the crystal outer surface and the temperature at the crystal center respectively] wherein the device has:

a control means for controlling an in-crystal temperature gradient in a pulling axis direction of the silicon single crystal ingot, and

a drive mechanism for moving the heat shielding element on the basis of an instruction from the control section.

9. (Twice Amended) A heat treating method for a relatively defect free silicon single crystal wafer related to a perfect crystal produced by a Czochralski method, characterized in that a heat treatment temperature at the initial entry of the silicon single crystal wafer to be a target of the heat treatment is 500°C or less, and a temperature ramping rate in a temperature range from the heat treatment temperature at initial entry to an ultimate temperature set in a range of 700°C - 900°C is set to 1°C/min or less.

10. (Twice Amended) A heat treating method for a relatively defect free silicon single crystal wafer related to a perfect crystal produced by a Czochralski method, characterized in that a heat treatment temperature at the initial entry of the silicon single crystal wafer to be a target of the heat treatment is 500°C or less, and a temperature ramping rate in a temperature range from the heat treatment temperature at initial entry to an ultimate temperature set in a range of 700°C -

900°C is set to 1°C/min or less, so as to make uniform the distribution of an oxide precipitate density of the silicon single crystal wafer after heat treatment.

11. (Twice Amended) A heat treating method for a relatively defect free silicon single crystal wafer related to a perfect crystal produced by a Czochralski method, characterized in that a heat treatment temperature at the initial entry of the silicon single crystal wafer to be a target of the heat treatment and a temperature ramping rate from the heat treatment temperature at initial entry to an ultimate temperature set in a range of 700°C - 900°C are adjusted so as to adjust the distribution of an oxide precipitate density of the silicon single crystal wafer after heat treatment.